# HERITAGE INSTITUTE OF TECHNOLOGY

TIME TABLE <ECE(VLSI)>

### M. Tech 1st Year 1st Semester

**SESSION: 2023-2024** 

DAY	9.00 AM – 9.55 AM	9.55 AM – 10.50 AM	10.50 AM – 11.45 AM	11.45 AM - 12.25 PM	12.25 PM – 1.20 PM	1.20 PM – 2.15 PM	2.15 PM – 3.10 PM	3.10 PM - 4.05 PM	4.05 PM – 5.00 PM	5.00 PM – 5.55 PM
MON	L/VLSI5101/K D/ICT614	L/VLSI5132/TC/IC T614	L/VLSI5102/SJ C/ICT614		MENTORIN G/ICT 614					
TUE	L/VLSI5102/SJ C/ICT614	L/VLSI5142/SP/ICT 614	LIBRARY							
WED	L/VLSI5101/KD/ICT614 L/VLSI5142/SP /ICT614				LAB/VLSI5151/PS/ICT602/PS*					
THU	L/VLSI5132/T C/ICT614 L/ECEN5103/MK/ICT612					LAB/VLSI5152/AS/ICT602/AR*				
FRI	L/VLSI5102/SJ C/ICT614				L/VLSI5142/S P/ICT614	L/VLSI5 132/TC/I CT614				

To be Effective from the date of commencement of First year classes
A minimum of 75% attendance is mandatory for being eligible to sit for the End-Semester Examination
Students should target 100% attendance

Member W

HOD

Saralo Chen humi Principal

### HERITAGE INSTITUTE OF TECHNOLOGY

TIME TABLE <ECE(VLSI)>

### M. Tech 1st Year 1st Semester

SESSION: 2023-2024

INITIALS	FULLNAME	DEPT	INITIALS	FULLNAME	DEPT
KD	KRISHANU DUTTA	ECE	PS*	PRITAM SAHU	ECE
MK	MOUSIKI KAR	ECE	AR*	ADITI ROY	ECE
SJC	SUBHRAJIT CHAKRABORTY	ECE			
TC	TAPAS CHAKRABORTY	ECE			
SP	SRABANTI PANDIT	ECE			
PS	PRATIMA SHAW	ECE			
SR	SIULI ROY	IT			

To be Effective from the date of commencement of First year classes A minimum of 75% attendance is mandatory for being eligible to sit for the End-Semester Examination Students should target 100% attendance

Member 2

13

Princip

HOD

# HERITAGE INSTITUTE OF TECHNOLOGY

TIME TABLE <ECE(VLSI)>

M. Tech Year 1st Semester

SESSION: 2023-2024

**COURSE STRUCTURE:** 

COURSE STRUCTURE IN
M.Tech. VLSI
1st. Year, Semester I

Sl. No.	Course Type	Code	Course Title	Contact Hours/Week				Credits
				L	T	P	Total	
1	Professional core 1	VLSI5101	Digital VLSI IC Design	3	0	0	3	3
2	Professional core 2	VLS15102	Embedded Systems Design	3	0	0	3	3
3	Professional Elective	VLS15131	DSP For VLSI System	3	0	0	3	3
	PE-1	VLSI5132 VLSI IC Fabr	VLSI IC Fabrication		0			3
4	Professional Elective	VLSI5141	CAD of Digital System	. 3	0	0		20
	PE-2	VLSI5142	Modelling of VLSI Device		0		3	3
5	Mgt. Group	ECEN5103	Research Methodology and IPR	2	0	0	2	2
6	Audit I	DIMA5116	Disaster Management			-		
		INCO5117	Constitution of India					
	-	PDLS5118	Personality Development					
		YOGA5119	Stress Management by Yoga	2	2 0	0	2	0
		SANS5120	Sanskrit for Technical Knowledge					
Total of Theory			16	0	0	16	14	

B.	Practical			THE WAR				
1	Professional Core Lab1	VLS15151	Digital VLSI IC Design Lab	0	0	4	4	2
2	Professional Core Lab2	VLS15152	Embedded Systems Design Lab	0	0	4	4	2
Total of Practical				0	0	8	8	4
Total of Semester			16	0	8	24	18	

To be Effective from the date of commencement of First year classes
A minimum of 75% attendance is mandatory for being eligible to sit for the End-Semester Examination
Students should target 100% attendance

Member

Lady

HOD

Berale Charthuri Principal